REMARKS

Applicants respectfully request favorable reconsideration of this application as amended.

By the above amendment, Claim 14 has been clarified to recite that the conductive layer of the memory cell is formed as part of a same conductive layer as a gate electrode of an insulated gate field effect transistor in the peripheral circuit. This feature is illustrated in at least Figs. 11 and 12, and described in the corresponding portion of the specification on the bottom of page 31 and on page 33, lines 6-9.

The claims have also generally been amended for clarity with independent Claims 1, 2, 24, 25 and 26 have been amended to recite that a potential applied to the insulating layer enables movement of carriers through the multi-layer, and at least the plural semiconductor layers are disposed below a surface of the semiconductor substrate.

Independent Claim 3 has been amended to recite each memory cell has a multi-layer of a conductive layer, an insulating layer that enables a tunneling effect, and plural semiconductor layers containing impurities. The plural semiconductor layers are present in the

semiconductor substrate and are disposed below a surface of the semiconductor substrate.

Independent Claim 32 has been amended to recite that a current that flows when a potential is applied to the insulating layer is capable of moving carriers by way of the multi-layer and has a hysteresis characteristic relative to the applied voltage, wherein at least the plural semiconductor layers are disposed below a surface of the semiconductor substrate.

Claim 29 has been cancelled thus rendering the rejection of Claim 29 moot.

The Office Action rejected independent Claims 1, 2, 24, 25 and 32 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,034,882 to Johnson et al (hereinafter "Johnson"), independent Claim 3 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,904,518 to Komori et al (hereinafter "Komori") and independent Claim 26 under 35 U.S.C. § 103(a) as unpatentable over Komori. As will be appreciated from the following discussion, the claimed invention is patentably distinguishable from the cited references.

None of the references of record teaches or suggests a memory cell multi-layer having plural semiconductor layers

disposed below a surface of the semiconductor substrate in combination with the movement of carriers through the multi-layer, as recited in independent Claims 1, 2, 24, 25 and 26, or with an insulating layer that enables a tunneling effect as recited in independent Claim 3, or with an insulating layer that is capable of moving carriers by way of the multi-layer and has a hysteresis characteristic relative to the applied voltage as recited in independent Claim 32. As is readily apparent, the remaining claims depart even further from the references of record.

With all objections and rejections having been overcome, an early Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on June 17, 2004.

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Mitchell W. Shapiro